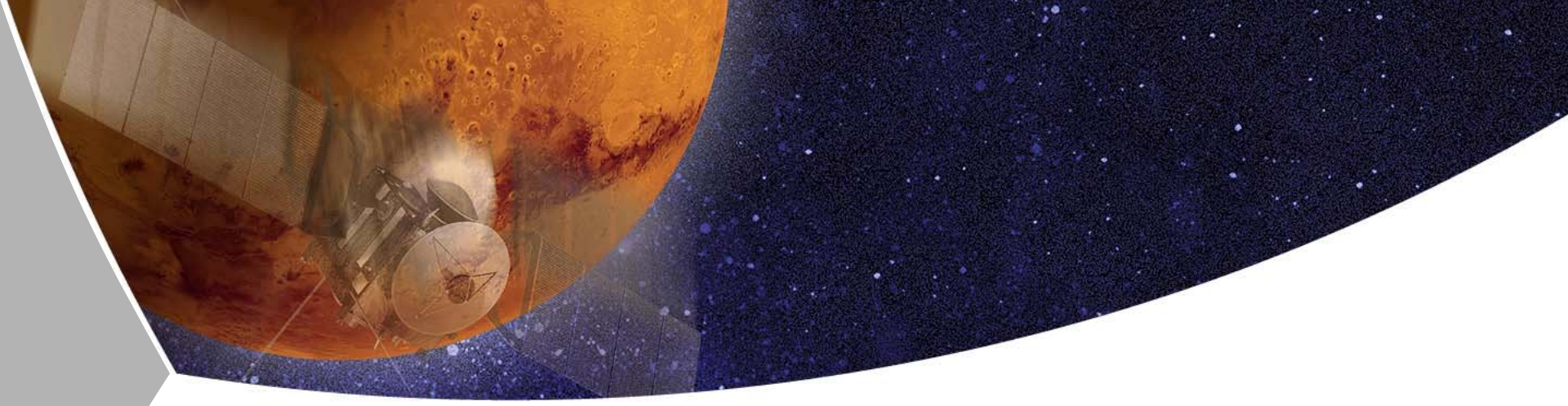


PLATO - Fast Telescope DPU Kick-Off Definition Phase

German Aerospace Center (DLR)

Institute of Robotics and Mechatronics

Department Optical Information Systems

G. Peter and the German PLATO Team

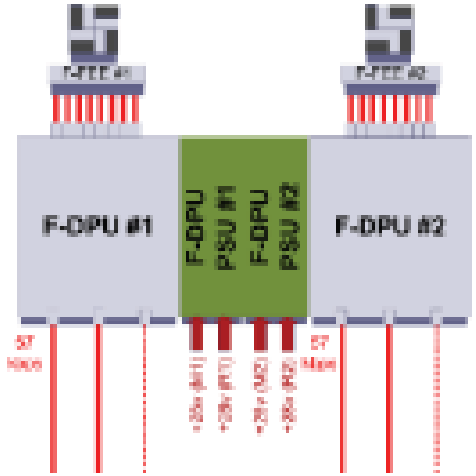
gisbert.peter@dlr.de, +493067055382

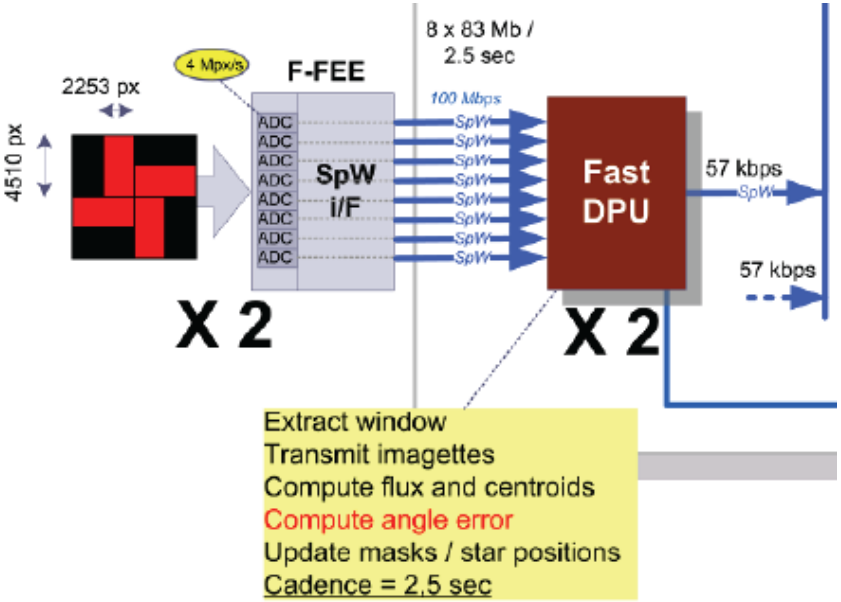
Deutsches Zentrum für Luft- und Raumfahrt e.V. in der Helmholtz-Gemeinschaft

EADS astrium

Tasks

- Fast Telescope Digital Processing Unit = F-DPU
- Control of F-FEE and acquisition of image data, 4 x frame transfer CCD á 2253 x 4510 pixels / 2,5sec
- Bright stars data processing
- Data extraction from F-FEE images
- Data correction (smearing, offset, background, gain)
- Providing angle/pointing error and barycenter data to SVM AOCS with low delay ensuring high accurate S/C pointing
- Science data processing providing intensity, centroids, imagetts to ICU
- Providing F-FEE and F-DPU housekeeping and status data
- Power supply of F-DPU

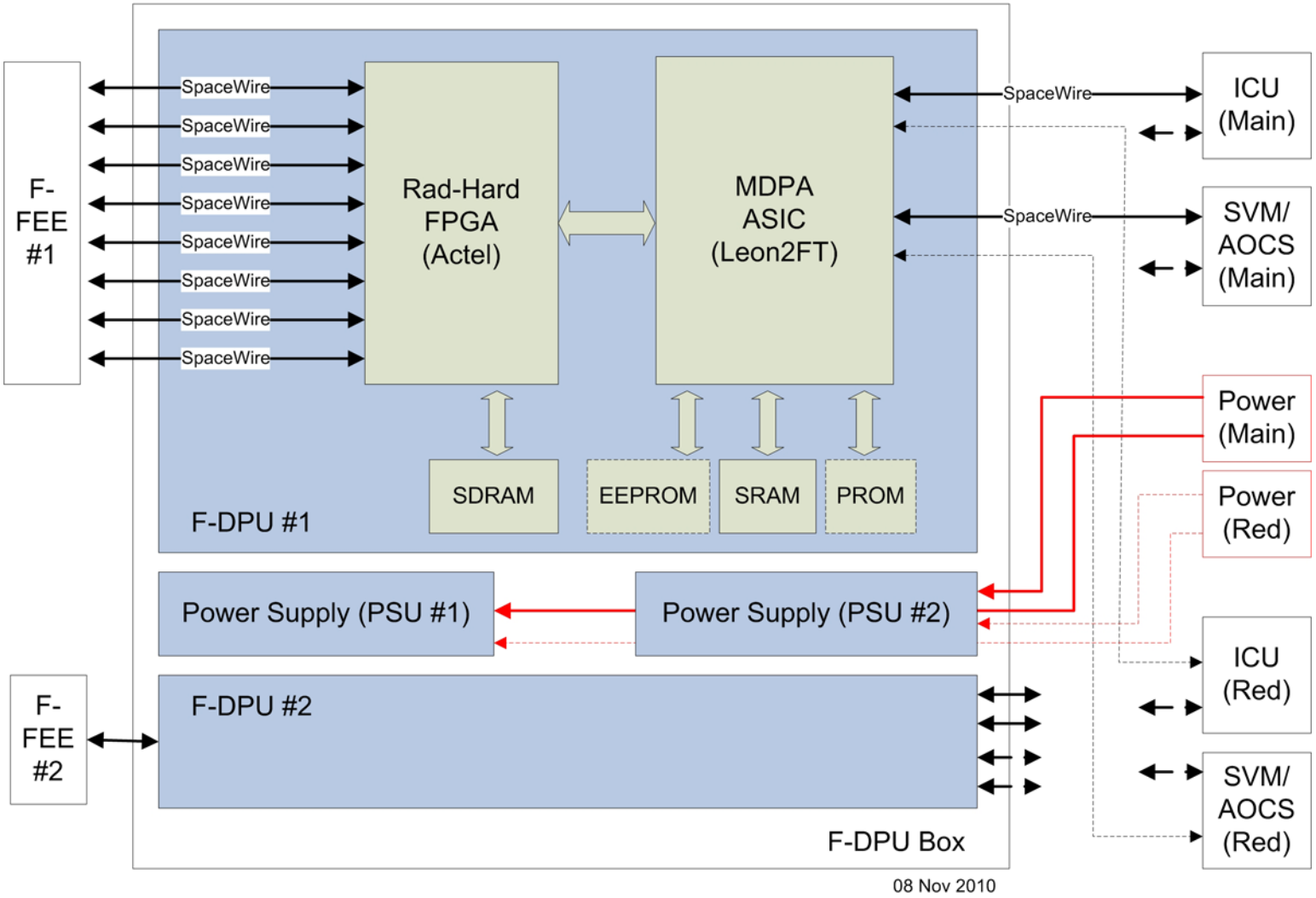




Design Driver

- High reliability of continuous operation over 6+2 years (2-3 year pointing phases)
- High precision of light curves and barycenter/error angles processing
- Fast data acquisition / high data amount from F-FEE (read out within 0,8sec → 600Mbps)
- Low delay of error angle calculation

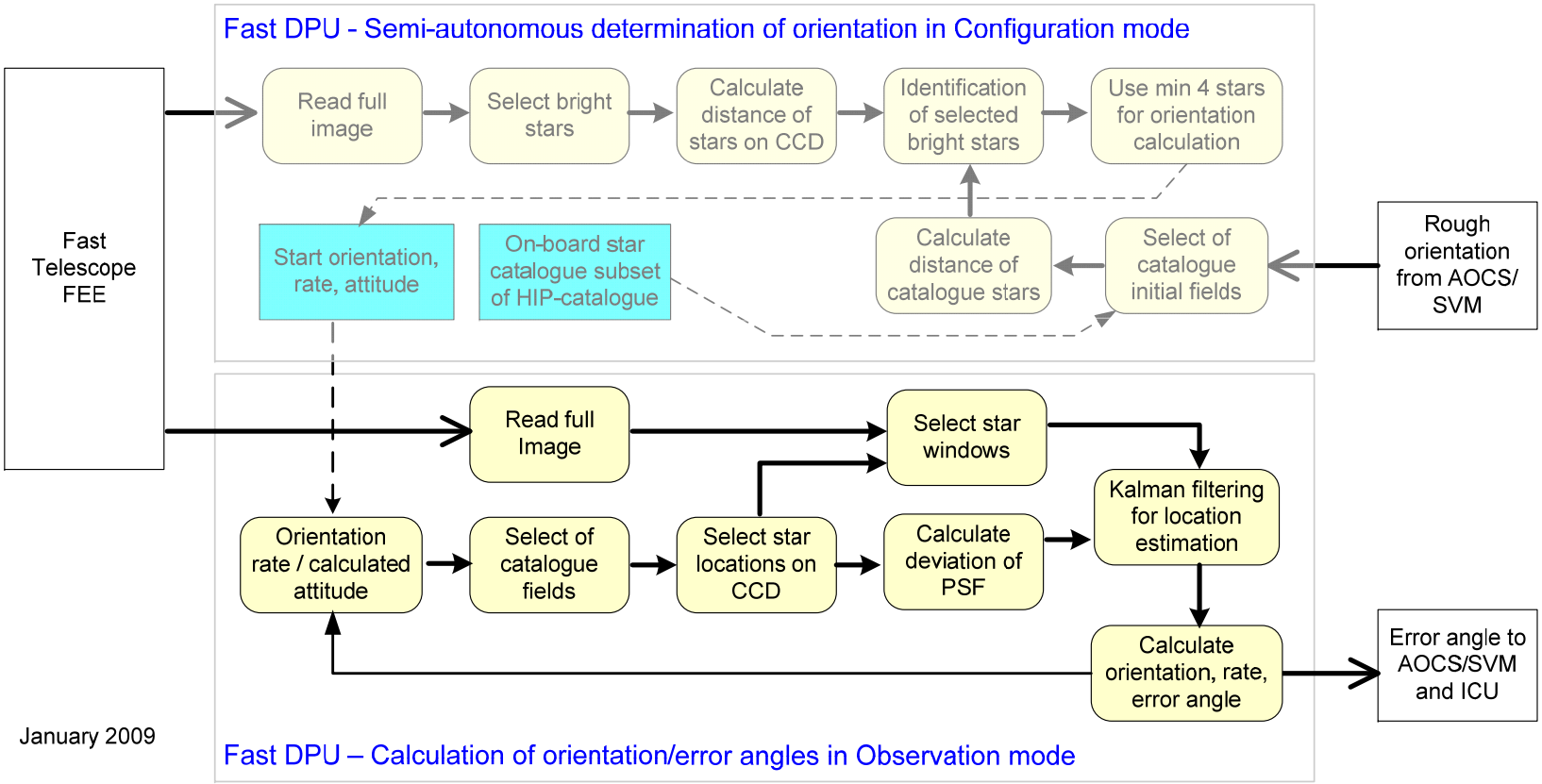
Architecture Design



Architecture Characteristics

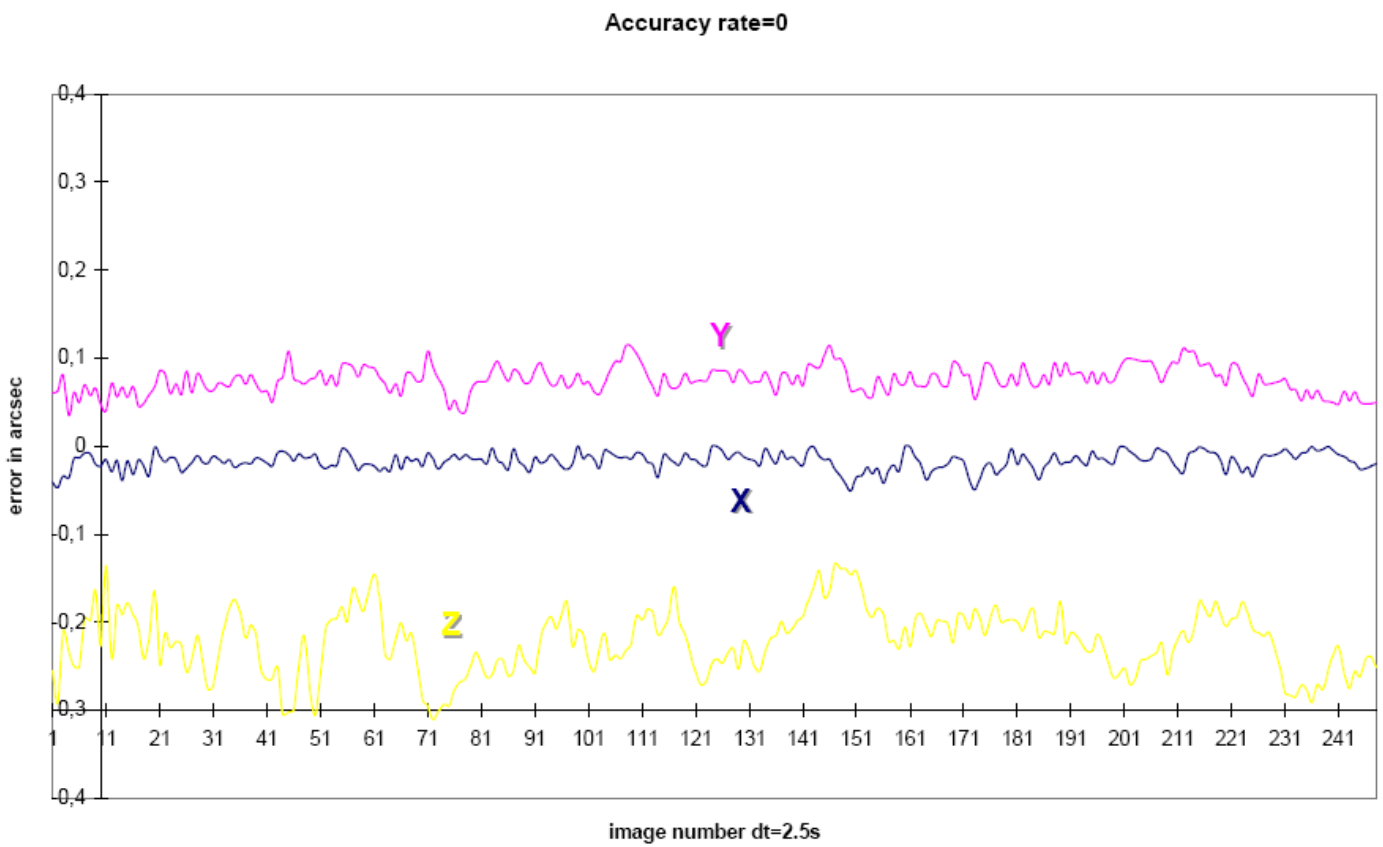
- Main and hot redundant DPU and power supply within one single box
- Main and redundant units electrically independent to each other
- ASIC incl. LEON2FT core and FPU (up to 80MHz)
- Fast SRAM for processing (> 8MByte, 0 wait states)
- FPGA for high speed F-FEE data acquisition
- SDRAM for image data storage (> 500MByte)
- EEPROM for storing on-board software and parameters (> 2 MByte)
- Spacewire for ICU and AOCS communication (4 x 10Mbit/s)
- Spacewire for F-FEE communication (8 x 100Mbit/s)
- Technological interfaces for development and test purposes
- On-board timer and FEE synchronization via Spacewire time code
- Supporting RMAP to software/parameter upload from ICU

Processing Architecture – Error Angle Calculation



Assessment Study Result (nominal error < 0.1 arcsec)

With Gaussian PSF

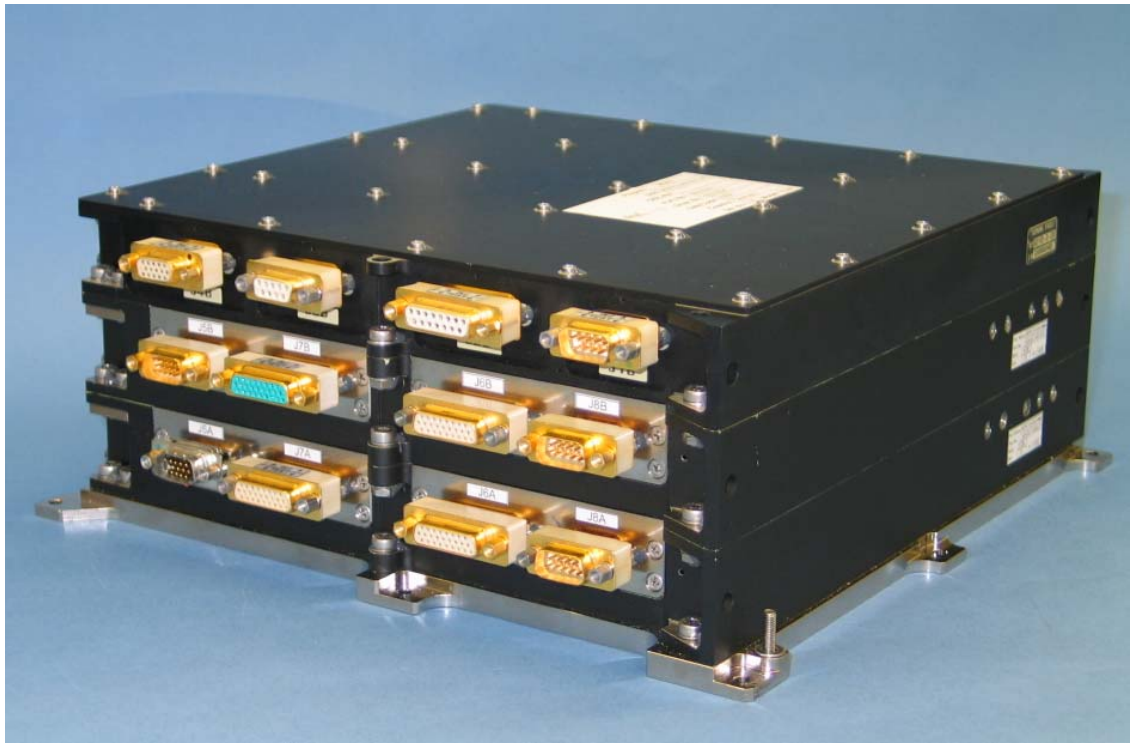


On-Board Software

- Primary boot software (PROM) → Software maintenance
- Optional: upload from ICU via SpaceWire RMAP protocol
- Application software (EEPROM)
- RTOS RTEMS
- Collection housekeeping and status information
- heath check and error handling
- F-FEE control and data read-out synchronization
- Control of data acquisition
- Scientific and pointing data processing
- Packing of results and data transfer to ICU (CCSDS) and AOCS
- Mode control (safe, configuration, observation, calibration)
- Size of Application software about 300kbyte

Example of DPU design

- Mass < 4,5kg + contingency
- Power consumption < 20 W



Verfication

Function, Accuracy, Real-time performance of algorithms / software

- Simulation of F-FEE images and stars considering realistic optical and CCD performance and disturbance
- Pre-validation with data provided by the PLATO simulator
- ICU and AOCS interface simulator
- Software and Hardware in the loop simulation

Function and performance of hardware

- Following ESA ECSS requirements
- Reliability, FMECA, derating analysis
- Thermal and Structural analysis
- TV and vibration tests

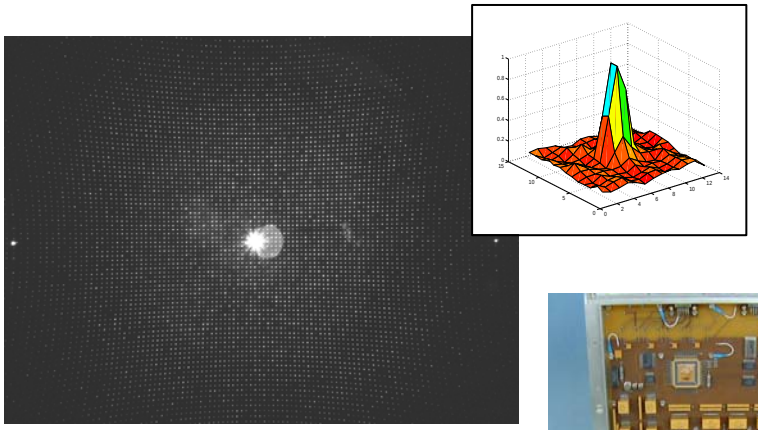
Model Philosophy

- **STM** box incl. 2 x F-DPU and 2 x PSU dummies (delivery)
- **EM** box incl. 1 x F-DPU and 1 x F-PSU for design validation and coupling tests with other equipments (delivery)
- **EM** box incl. 1 x F-DPU and 1 x F-PSU for development and test purposes (remain at DLR)
- **QM** box incl. 1 x F-DPU and 1 x F-PSU for qualification purposes and as fligth spare on board level (delivery on request) plus 1 x F-DPU and 1 x F-PSU dummies (delivery)
- **FM** box incl. 2 x F-DPU and 2 x F-PSU (delivery)

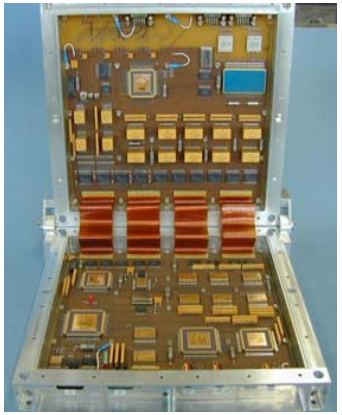
Tasks of Definition Phase

- Analysis/simulation of Precision of data processing with realistic disturbance and optical distortion characteristics
- Hardware and software prototyping
- Detailed of operational concept and modes
- Definition of hardware architecture, interface and prel. design
- Definition of software architecture, interface and prel. design definition
- Definition of development and verification plan for next phases

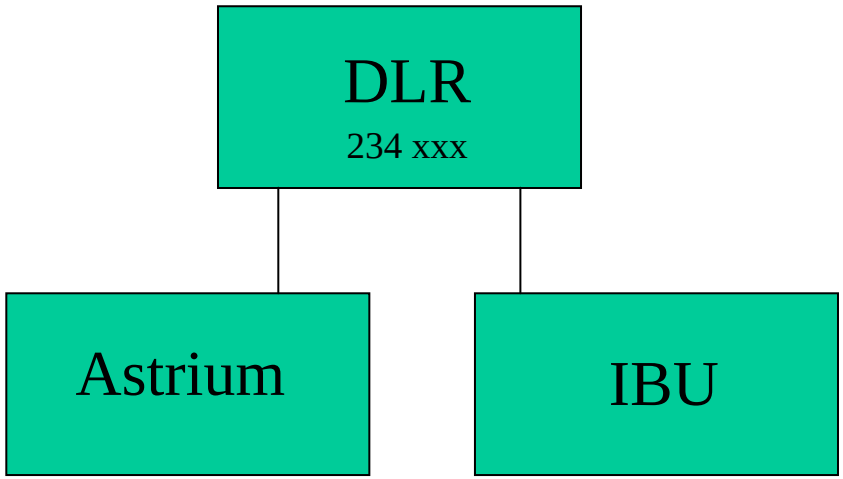
Organization



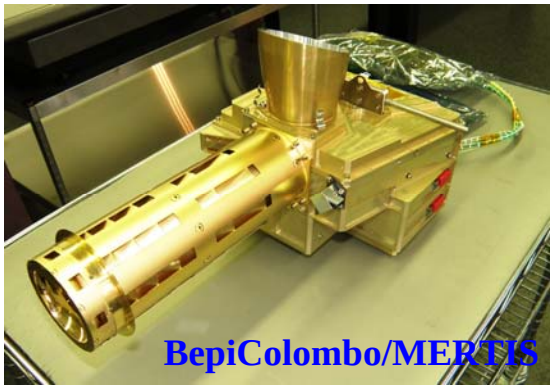
Optical Navigation & Calibration



COROT/DPU



- DLR : management, algorithms, verification
- Astrium: Hardware design, prototyping, verification
- IBU : software design, prototyping



BepiColombo/MERTIS

Thanks